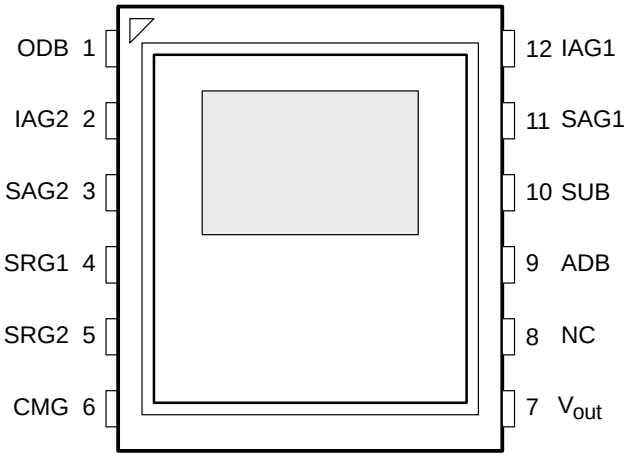
- **Very Low Noise, High Sensitivity, Electronically Variable**
- **High Resolution, 1/3-in Format, Solid State Charge-Coupled Device (CCD) Frame Transfer Image Sensor for Black and White National Television and Standard Committee (NTSC) and Computer Applications**
- **340,000 Pixels per Field**
- **Frame Memory**
- **656 (H) × 496 (V) Active Pixels in Image Sensing Area Compatible With Electronic Centering**
- **Multimode Readout Capability**
  - **Progressive Scan**
  - **Interlace Scan**
  - **Line Summing**
- **Fast Single-Pulse Clear Capability**
- **Continuous Electronic Exposure Control from 1/60 s to 1/5,000 s**
- **7.4 μm Square Pixels**
- **Advanced Lateral Overflow Drain**
- **Low Dark Current**

DUAL-IN-LINE PACKAGE
(TOP VIEW)



- **High Photoresponse Uniformity from Deep Ultraviolet (DUV) to Near Infrared (NIR)**
- **Solid State Reliability With No Image Burn-In, Residual Imaging, Image Distortion, Image Lag, or Microphonics**

ADVANCE INFORMATION

description

The TC253SPD device is a frame-transfer, CCD image sensor designed for use in black and white NTSC TV, computer, and special-purpose applications that require high sensitivity, low noise, and small size.

The TC253SPD sensor is a new device of the IMPACTRON™ family of very low noise, high sensitivity image sensors that multiply charge directly in the charge domain before conversion to voltage. The charge carrier multiplication (CCM) is achieved by using a low-noise, single-carrier, impact ionization process that occurs during repeated carrier transfers through high field regions. Applying multiplication pulses to specially designed gates activates the CCM. The amount of multiplication is adjustable, depending on the amplitude of the multiplication pulses. The device function resembles the function of image intensifiers implemented in solid state.

This MOS device contains limited built-in gate protection. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to V_{SS}. Under no circumstances should pin voltages exceed absolute maximum ratings. Avoid shorting OUT to V_{SS} during operation to prevent damage to the amplifier. The device can also be damaged if the output terminals are reverse-biased and an excessive current is allowed to flow. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

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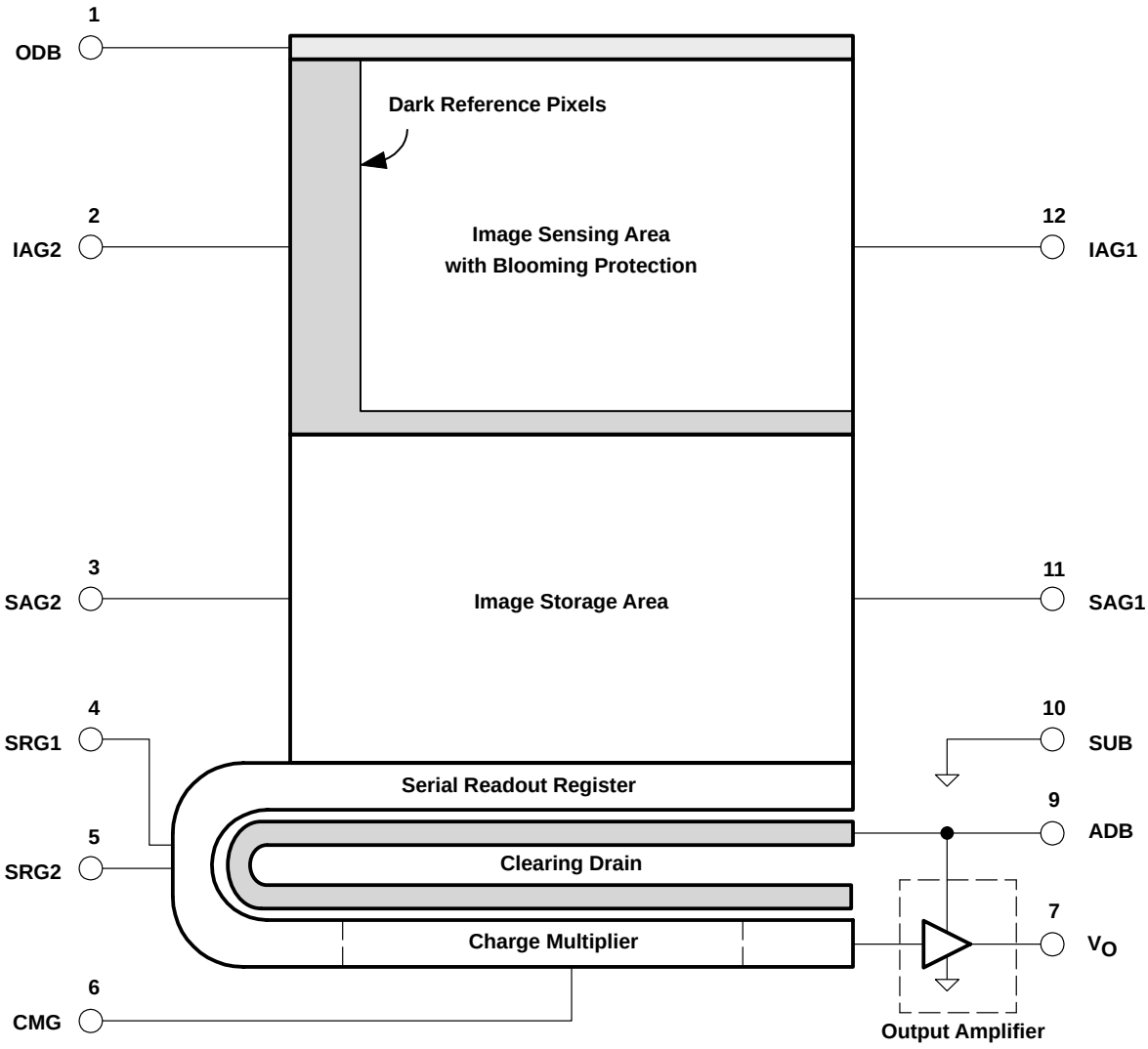
description (continued)

The image-sensing area of the TC253SPD sensor is configured into 500 lines with 680 pixels in each line. Twenty-two pixels are reserved in each line for dark reference. The blooming protection is based on an advanced lateral overflow drain concept that does not reduce NIR response. The sensor can be operated in the interlaced or progressive scan modes and can capture full 340,000 pixels in one image field. The frame transfer from the image-sensing area to the memory area is accomplished at a very high rate that minimizes image smear. The electronic exposure control is achieved by clearing unwanted charge from the image area using a short positive pulse applied to the antiblooming drain. This pulse marks the beginning of the integration time, which can be arbitrarily shortened from its nominal length. After charge is integrated and stored in the memory it is available for readout in the next cycle. This is accomplished using a unique serial register design that includes special charge multiplication pixels.

The TC253SPD sensor is built using TI-proprietary advanced split-gate virtual-phase CCD (SGVPCCD) technology, which provides devices with wide spectral response, ranging from DUV to NIR, high quantum efficiency (QE), low dark current, and high response uniformity. The TC253SPD sensor is characterized over an operating free-air temperature range of T_A= –10°C to 45°C.

functional block diagram



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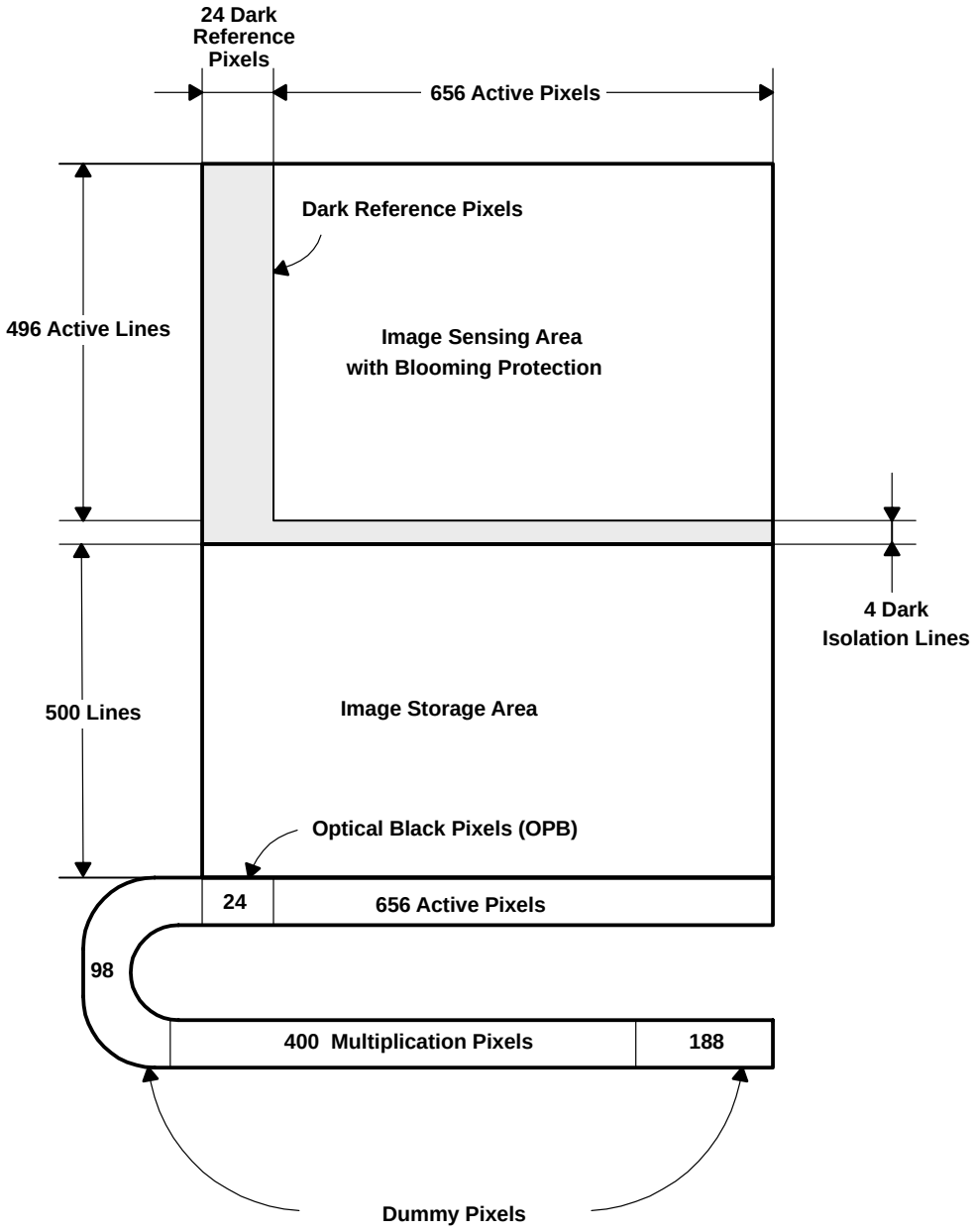
sensor topology diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADB	9	I	Supply voltage for amplifiers and clearing drain
CMG	6	I	Charge multiplication gate
IAG1	12	I	Image area gate 1
IAG2	2	I	Image area gate 2
NC	8	–	No connection
ODB	1	I	Supply voltage for antiblooming drain
V_{OUT}	7	O	Output signal, multiplier channel
SAG1	11	I	Storage area gate 1
SAG2	3	I	Storage area gate 2
SRG1	4	I	Serial register gate 1
SRG2	5	I	Serial register gate 2
SUB	10		Chip substrate

detailed description

The TC253SPD sensor consists of four basic functional blocks: the image-sensing area, the image storage area, the serial register, and the charge multiplier. The location of each of these blocks is identified in the functional block diagram.

image-sensing and storage areas

Figure 1 and Figure 2 show cross sections with potential-well diagrams and top views of the pixels in the image-sensing and storage areas. As light enters silicon in the image-sensing area, electrons are generated and collected in potential wells of the pixels. Applying a suitable dc bias to the antiblooming drain provides blooming protection. Electrons that exceed a specified level, determined by the ODB bias, are drained away from the pixels. If it is necessary to remove all previously accumulated charge from the wells, a short positive pulse must be applied to the drain. This marks the beginning of the new integration period. After the integration cycle is completed, charge is quickly transferred into the memory where it waits for readout. The lines can be read out from the memory in a sequential order to implement progressive scan, or two lines can be summed together to implement the pseudo-interlace scan.

Twenty-two columns at the left edge of the image-sensing area are shielded from incident light. These pixels provide the dark reference used in subsequent video-processing circuits to restore the video black level. An additional four dark lines located between the image-sensing area and the image storage area were added for isolation.

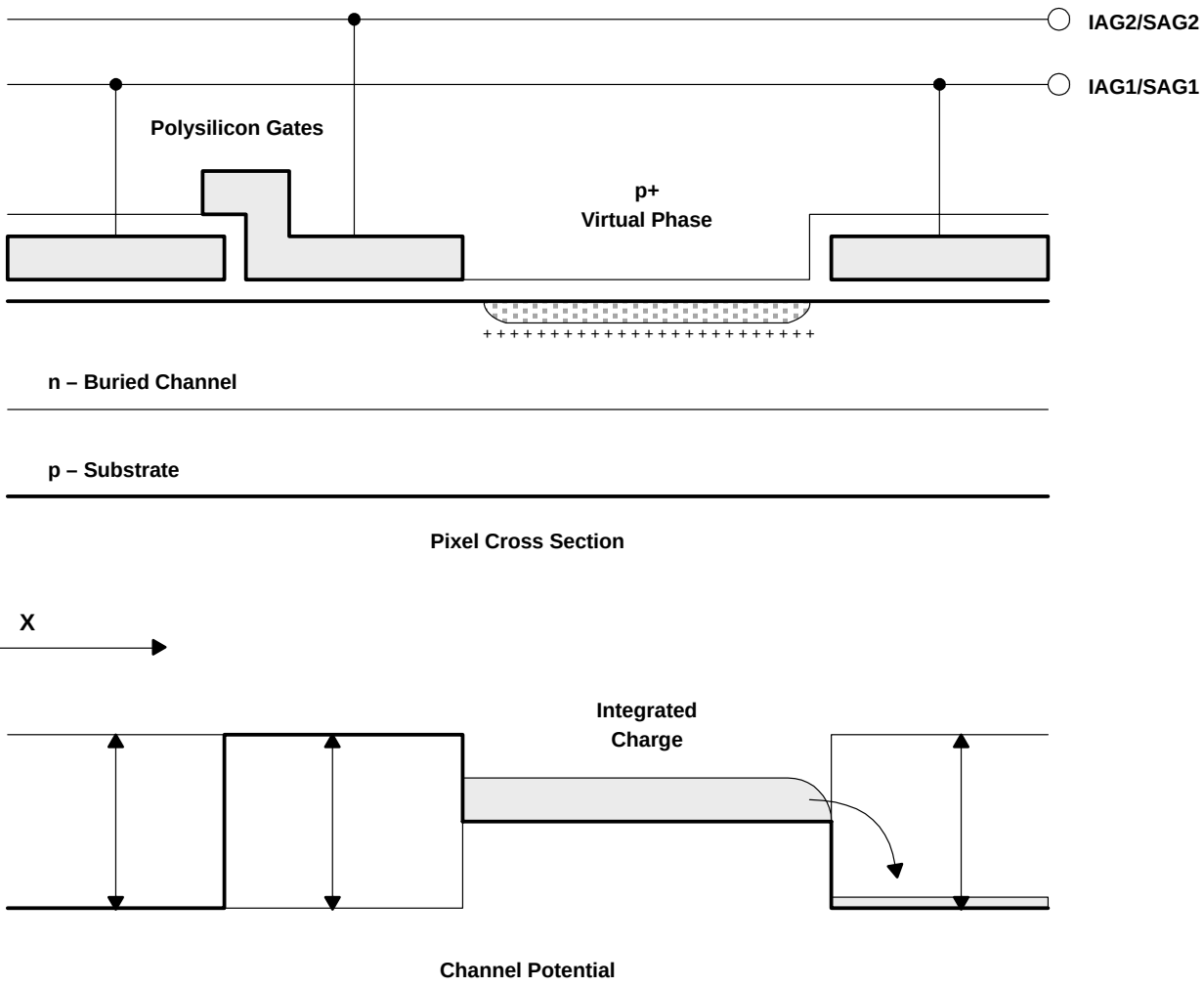


Figure 1. Image Area and Storage Area Pixel Cross Section with Channel Potential

ADVANCE INFORMATION

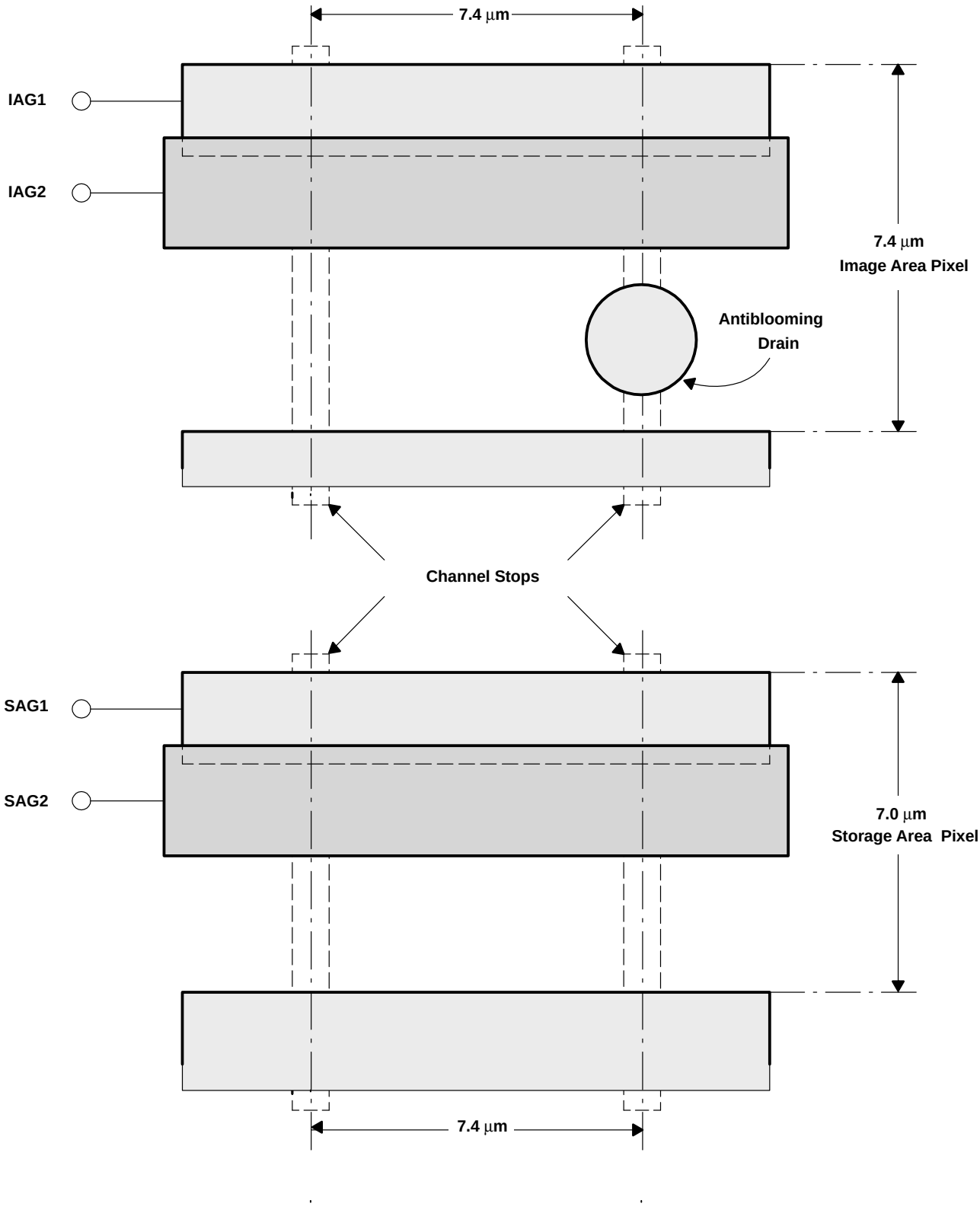


Figure 2. Image Area and Memory Area Pixel Topologies

advanced lateral overflow drain

The advanced lateral overflow drain structure is shared by two neighboring pixels in each line. Varying the dc bias of the antiblooming drain can control the blooming protection level and trade it for well capacity. Applying a pulse (approximately 10 V above the nominal level for a minimum of 1 μs) to the drain removes all charge from the pixels. This feature permits a precise control of the integration time on a frame-by-frame basis. The single-pulse clearing capability also reduces smear by eliminating accumulated charge in the pixels before the start of the integration period (single-sided smear). The application of a negative 1-V pulse to the antiblooming drain during the parallel transfer is recommended. This pulse prevents creation of undesirable artifacts caused by the on-chip crosstalk between the image area gate clock lines and the antiblooming drain bias lines.

serial register and charge multiplier

The serial register is used to transport charge stored in the pixels of the memory to the output amplifier. However, the TC253SPD device has a serial register with twice the standard length. The first half has a conventional design that interfaces with the memory and the clearing drain as it would in any other CCD sensor (for example the TC237 sensor). The second half, however, is unique and includes 400 charge multiplication stages with a number of dummy pixels that are needed to transport charge between the active register blocks and the output amplifier. Charge is multiplied as it progresses from stage to stage in the multiplier toward the charge detection node. The charge multiplication level depends on the amplitude of multiplication pulses (approximately 11 V ~ 17 V) applied to the multiplication gates. Due to the double length of the registers, the first line in the field or frame scan does not contain valid data and must be discarded.

readout and video processing

The last element of the charge readout and detection chain is the charge detection node. Charge detection nodes use standard floating diffusion (FD) concepts followed by dual-stage source followers as buffer amplifiers. The reset gate is internally connected to SRG1. This connection results in a simultaneous FD reset when the SRG1 gate is clocked high. To achieve the ultimate sensor performance, it is necessary to eliminate the detection node kTC noise using CDS processing techniques. The IMPACTRON™ devices can detect single photons when cooling or when sufficiently short integration times are used.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{SS}: ADB (see Note 1) . . . . . SUB to SUB + 15 V
Supply voltage range, V_{SS}: ODB . . . . . SUB to SUB + 22 V
Input voltage range, V_I: IAG1, IAG2, SAG, SRG . . . . . –10 V to 10 V
Input voltage range, V_I: IAG1, SAG, SRG2 . . . . . –8 V to 8 V
Input voltage range, V_I: SRG1 . . . . . –5 V to 8 V
Input voltage range, V_I: CMG . . . . . –5 V to 15 V
Operating free-air temperature range, T_A . . . . . –10°C to 45°C
Storage temperature range, T_{stg} . . . . . –30°C to 85°C
Operating case temperature range, T_C . . . . . –10°C to 55°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to SUB.

recommended operating conditions

				MIN	NOM	MAX	UNIT
Substrate bias, V_{SS}					0		V
Supply voltage, V_{DD}	ADB				12		V
	ODB	For blooming control			6		
		For clearing			13		
		For transfer			5.5		
Input voltage, V_I†		IAG1	High		2.4		V
			Low		–3.2		
		IAG2	High		4.5		
			Low		–6.2		
		SAG1	High		2.4		
			Low		–2.4		
		SAG2	High		3.1		
			Low		–4.2		
		SRG1	High		4.2		
			Low		–4.6		
		SRG2	High		5.7		
			Low		–3.4		
		CMG	High	7	13.6		
			Low		–2		
Clock frequency, f_{clock}		IAG1, IAG2			3.125		MHz
		SAG1, SAG2			3.125		
		SRG1, SRG2			12.5		
		CMG			12.5		
Load capacitance		OUT				6	pF
Operating free-air temperature, T_A				–10		45	°C

† Fine tuning of input voltages is required in order to obtain good charge transfer.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER		MIN	TYP†	MAX	UNIT
	Charge multiplication gain		1	30	(100)‡	
	Charge multiplication gain temperature coefficient					%/°C
	Excess noise factor for typical CCM gain (see Note 2)		1	1.2	1.4	
	Dynamic range without CCM gain			58		dB
	Dynamic range with typical CCM gain (see Note 3)			50		dB
	Charge conversion gain without CCM (see Note 4)			10		μV/e
τ	Signal-response delay time (see Note 5)			9		ns
	Output resistance			320		Ω
	Amplifier noise-equivalent signal without CCM gain §			42		e
	Amplifier noise-equivalent signal with typical CCM gain §			1.5		e
	Response linearity with no CCM gain			1		
	Response linearity with typical CCM gain			1		
	Charge-transfer efficiency (see Note 6)		0.9998	0.9999		
	Supply current		2	3	4	mA
C_i	Input capacitance	IAG-1		2.95		nF
		IAG-2		3.22		
		IAG-1–IAG2		1.98		
		SAG-1		3.04		
		SAG-2		3.62		
		SAG-1–SAG2		2.22		
		SRG-1		40		pF
		SRG-2		40		
		SRG-1–SRG2				
		CMG		30		
		CMG–SRG1				
		ODB		1,000		
	Pulse amplitude rejection ratio	ADB high (see Note 7)		20		dB
		SRG-1, 2 high (see Note 7)		45		
		SRG-1, 2 low (see Note 7)		45		
		CMG high (see Note 7)		45		
		CMG low (see Note 7)		45		
		ODB low (see Note 7)		45		

† All typical values are at T_A = 25°C.
‡ Maximum CCM gain is not ensured.
§ The values in this table are quoted using correlated double sampling (CDS), which is a signal processing technique that improves performance by minimizing undesirable effects of reset noise.

NOTES:
2. Excess noise factor F is defined as the ratio of noise sigma after multiplication divided by M times the noise sigma before multiplication where M is the charge multiplication gain.
3. Dynamic range is –20 times the logarithm of the mean noise sigma divided by the saturation output signal amplitude.
4. Charge conversion factor is defined as the ratio of output signal to input number of electrons.
5. Signal-response delay time is the time between the falling edge of the SRG2 pulse and the output signal valid state.
6. Charge transfer efficiency is 1 minus the charge loss per transfer in the CCD register. The test is performed in the dark using either electrical or optical input.
7. Rejection ratio is –20 times the logarithm of the output referenced to the reset level divided by the 1 V of amplitude change of the corresponding gate or terminal signal.

optical characteristics, T_A = 40°C (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
	Sensitivity with typical CCM gain (see Note 8)	No IR filter		240		V/Lux
		With IR filter		33		
	Sensitivity without CCM gain (see Note 8)	No IR filter		8		V/Lux
		With IR filter		1.1		
V_{sat}	Saturation signal output no CCM gain (see Note 9)			260		mV
V_{sat}	Saturation signal output with typical CCM gain (see Note 9)			440		mV
V_{off}	Zero input offset output (see Note 10)			200		mV
	Blooming overload ratio (see Note 11)			1000:1		
	Image area well capacity			26k		
	Smear (see Note 12)				66	dB
	Dark current (see Note 13)		0.15	0.90		nA/cm^2
	Dark signal (see Note 14)		0.08	0.50		mV
	Dark-signal uniformity (see Note 15)		0.3			mV
	Dark-signal shading (see Note 16)		0.4			mV
	Spurious nonuniformity	Dark	0.8			mV
		Illuminated	–20%		20%	
	Column uniformity (see Note 17)		0.2			mV
	Electronic-shutter capability		1/5000	1/60		s

NOTES: 8. Light source temperature is 2856°K. The IR filter used is CM500 1 mm thick.
9. Saturation is the condition in which further increase in exposure does not lead to further increases in output signal.
10. Zero-input offset is the residual output signal measured from the reset level with no input charge present. This level is not caused by the dark current and remains approximately constant, independent of temperature. This level can vary with the amplitude of SRG2.
11. Blooming is the condition in which charge induced by light in one element spills over to the neighboring elements.
12. Smear is the measure of error signal introduced into the pixels by transferring them through the illuminated region into the memory. The illuminated region is 1/10 of the image area height. The value in the table is obtained for the integration time of 16.66 ms and 3.125 MHz vertical clock transfer frequency.
13. Dark current depends on temperature and approximately doubles every 8°C. Dark current is also multiplied by the CCM operation. The value given in the table is with the multiplier turned off, and it is a calculated value.
14. Dark signal is actual device output measured in darkness.
15. Dark signal uniformity is the sigma of difference of two neighboring pixels taken from all the image area pixels.
16. Dark signal shading is the difference between maximum and minimum of a 5-pixel median taken anywhere in the array.
17. Column uniformity is obtained by summing all the lines in the array, finding the maximum of the difference of two neighboring columns anywhere in the array, and dividing the result by the number of lines.

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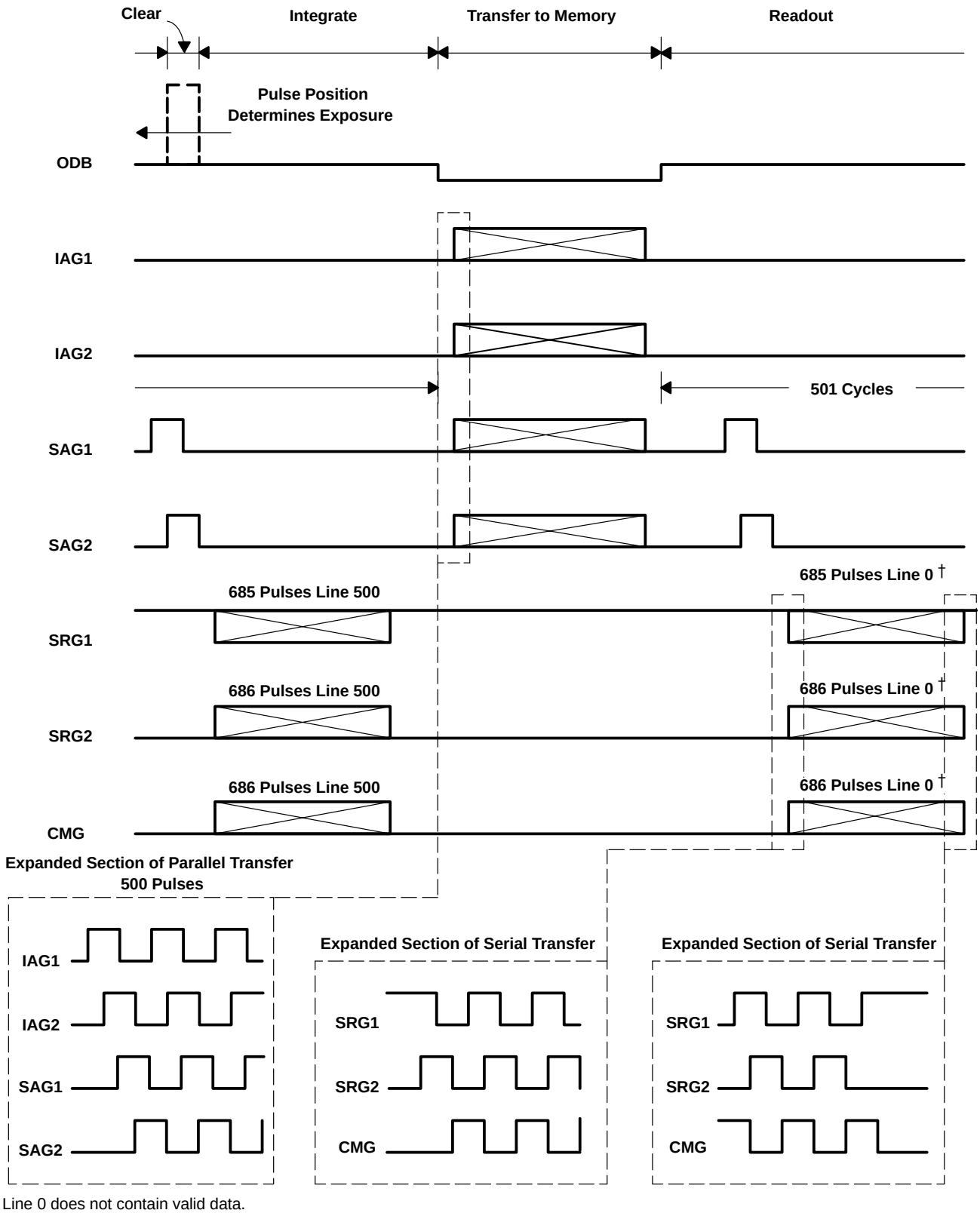
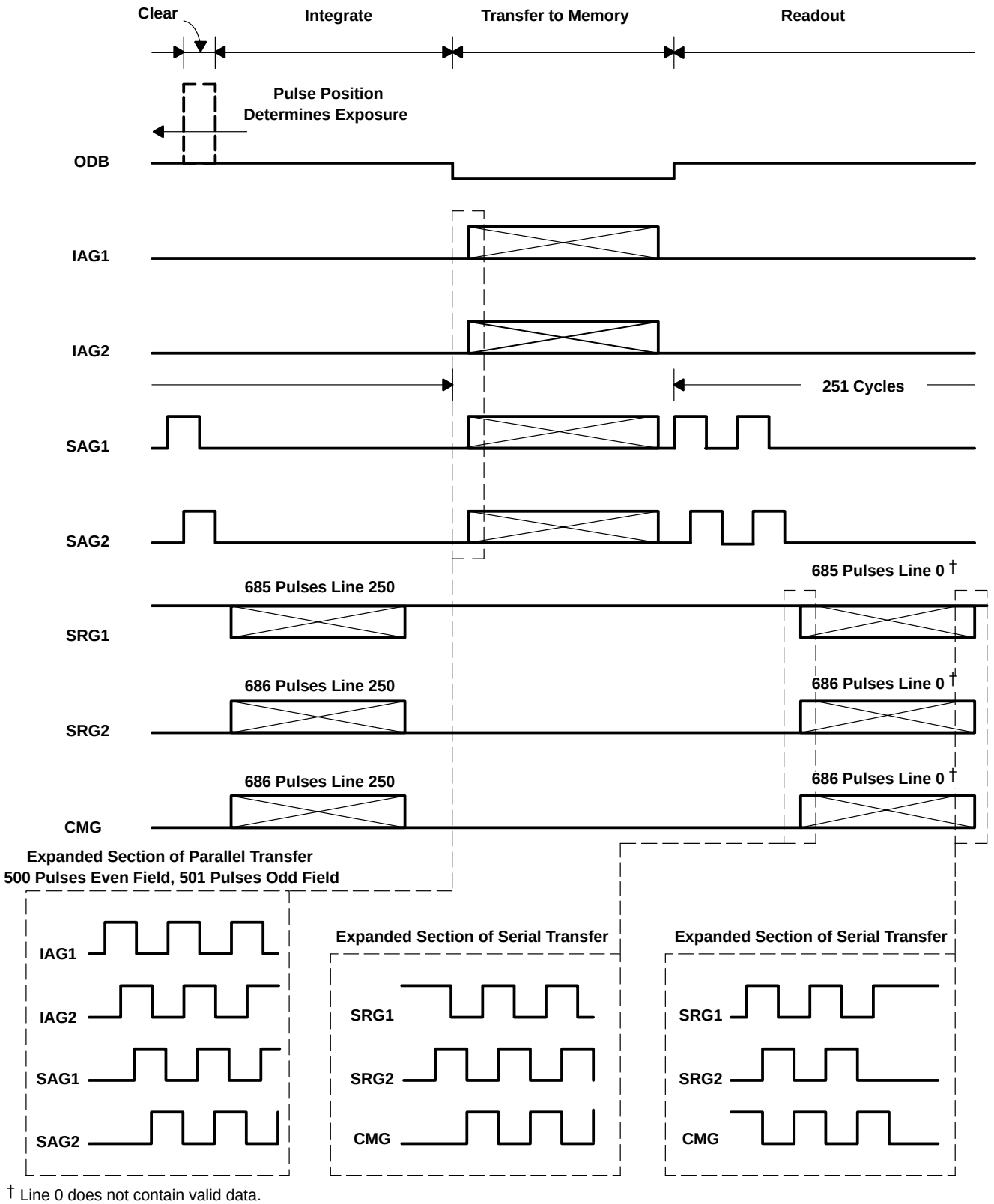


† Line 0 does not contain valid data.

Figure 3. Progressive Scan Timing



† Line 0 does not contain valid data.

Figure 4. Interlace Timing for Line Summing Mode

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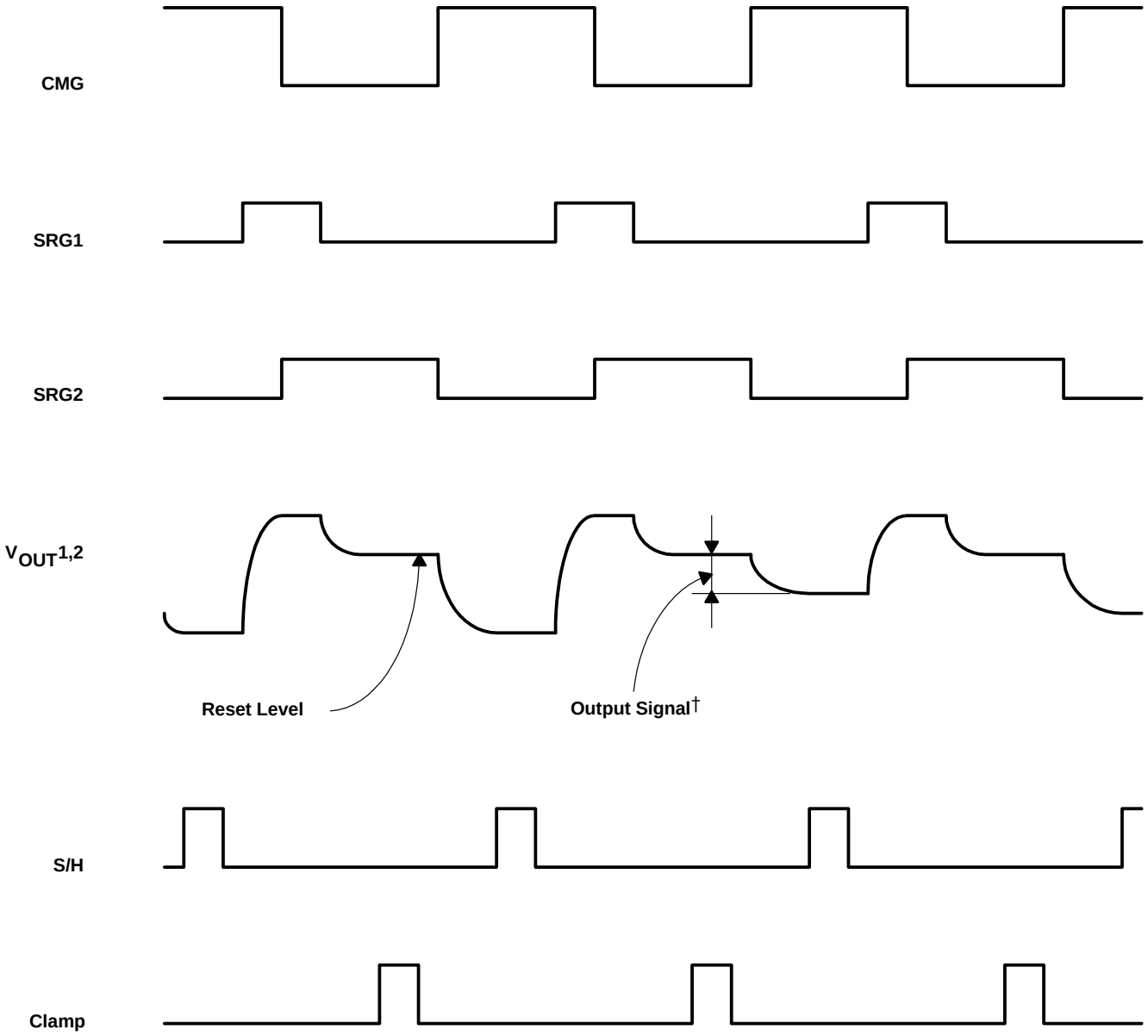

† Output signal may not be zero for zero-input charge. Offset level up to 100 mV may be present.

Figure 5. Detail Serial Register Clock Timing for CDS Implementation

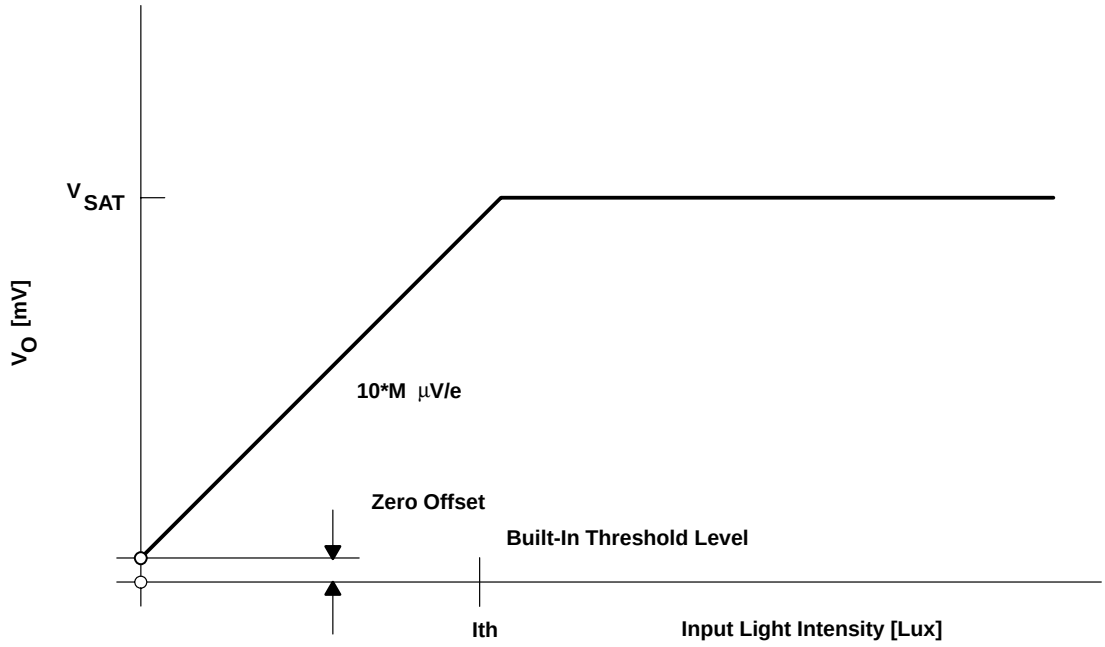

Figure 6. Photon Transfer Characteristic of CCD Outputs

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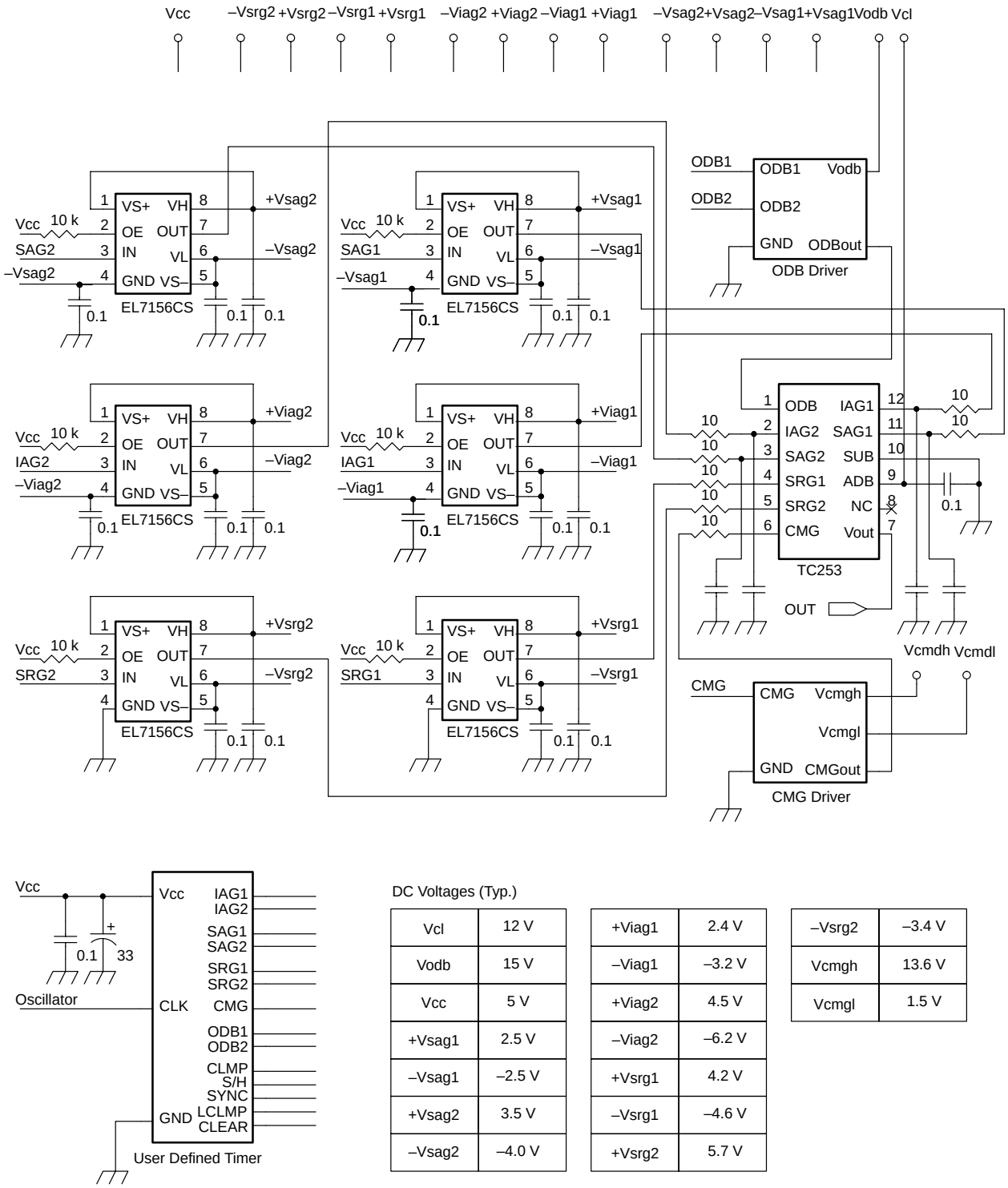


DC Voltages (Typ.)

Vcl	12 V
Vodb	15 V
Vcc	5 V
+Vsag1	2.5 V
–Vsag1	–2.5 V
+Vsag2	3.5 V
–Vsag2	–4.0 V

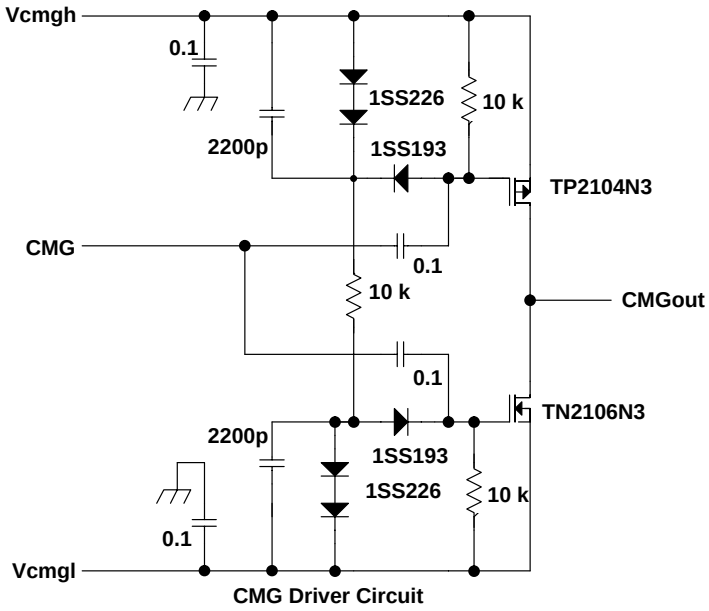
+Viag1	2.4 V
–Viag1	–3.2 V
+Viag2	4.5 V
–Viag2	–6.2 V
+Vsrg1	4.2 V
–Vsrg1	–4.6 V
+Vsrg2	5.7 V

–Vsrg2	–3.4 V
Vcmgh	13.6 V
Vcmgl	1.5 V

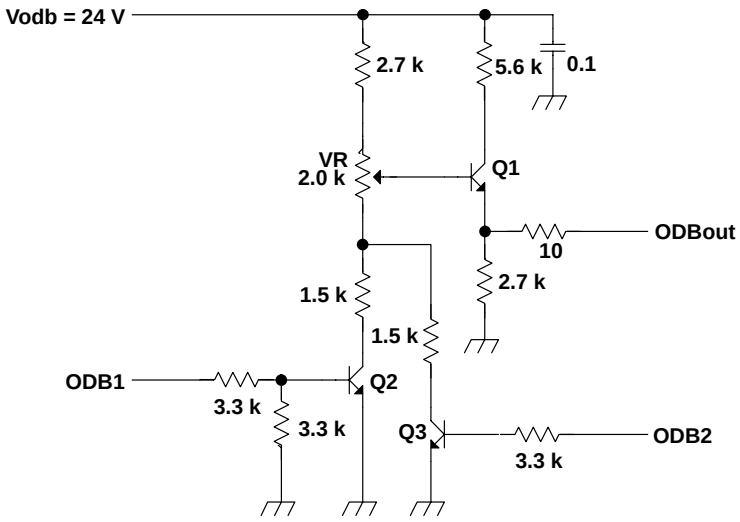
NOTES: A. All values are in Ω and μF unless otherwise noted.
B. TI recommends ac coupled system for coupling to the next video processing circuits.
C. IAG and SAG signal from user defined timer must be shifted its GND level to –V before the driver IC (EL7156CS) input.
D. The value of the CCD external capacitors (on IAG and SAG) were recommended with 2000 pF ~ 5000 pF.

Figure 7. Typical Application Circuit

APPLICATION INFORMATION



CMG Driver Circuit



ODB Driver Circuit

NOTE A: All values are in Ω and μF unless otherwise noted.

Figure 8. Example of CMG Driver Circuit

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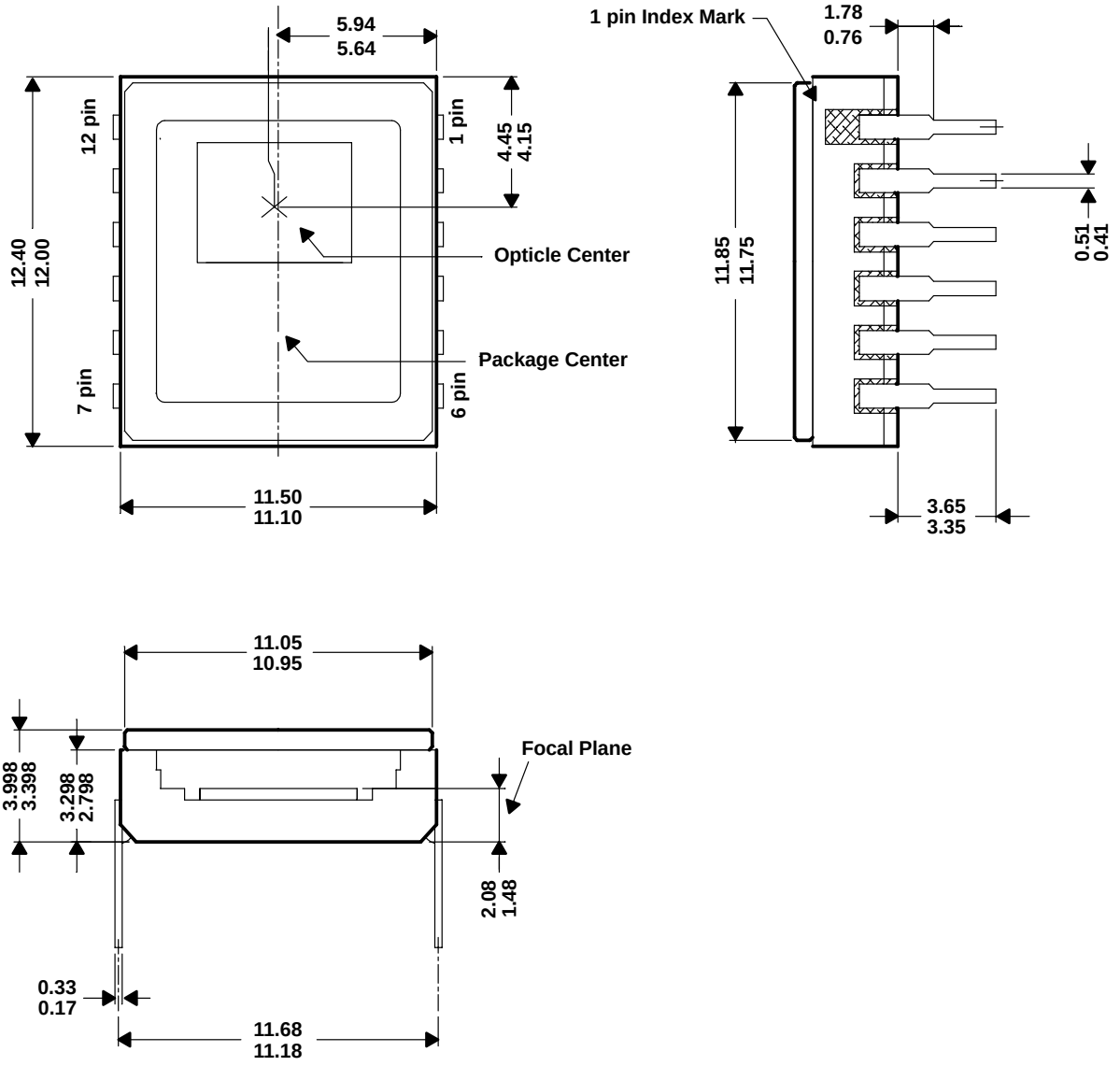
MECHANICAL DATA

The package for the TC253SPD image sensor consists of a ceramic base, a glass window, and a 12-lead frame. The glass window is sealed to the package by an epoxy adhesive. The package leads are configured in a dual-in-line arrangement and fit into mounting holes with 1,78 mm center-to-center spacing.

TC253 (12 pin)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS

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