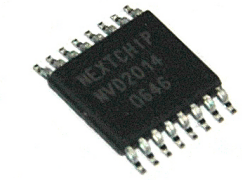
NVD2014

Data Sheet
Vertical Driver for 4-Phase CCD Sensors



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Description

: NVD2014 is a clock driver for 4-Phase CCD Image Sensor.

Features

-. 3 Levels Output Driver × 2
-. 2 Levels Output Driver × 2
-. 2 Levels Sub Driver × 1

Ordering Information

Device	Package	Temperature Range
NVD2014	16-TSSOP	- 20°C ~ + 85°C

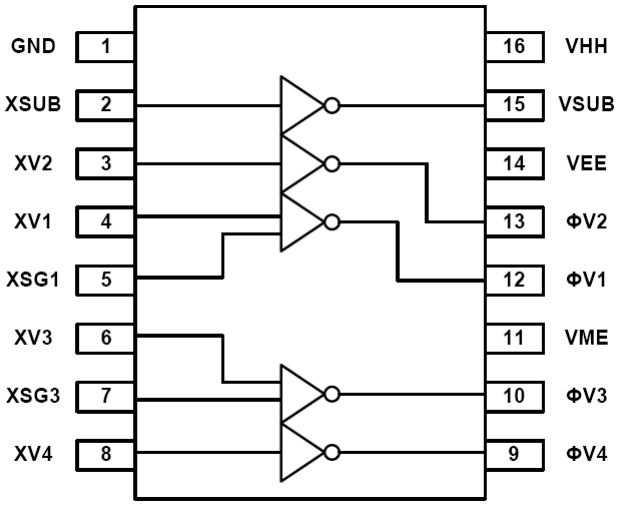
Applications

-. CCD Image Sensors

Related Products

-. NVD2004, NVD2006
-. NVP2000A, NVP2000E

Functional Block Diagram



[[Table of Contents]]

1. Pin Description

Pin	Symbol	I/O	Description	Remark
1	GND	-	Ground	
2	XSUB	I	Output Control (VSUB)	
3	XV2	I	Output Control (ΦV2)	
4	XV1	I	Output Control (ΦV1)	
5	XSG1	I	Output Control (ΦV1)	
6	XV3	I	Output Control (ΦV3)	
7	XSG3	I	Output Control (ΦV3)	
8	XV4	I	Output Control (ΦV4)	
9	ΦV4	O	High Voltage Output (2 level : VME, VEE)	
10	ΦV3	O	High Voltage Output (3 level : VME, VEE, VHH)	
11	VME	-	Power (0V)	
12	ΦV1	O	High Voltage Output (3 level : VME, VEE, VHH)	
13	ΦV2	O	High Voltage Output (2 level : VME, VEE)	
14	VEE	-	Power (-8.5V)	
15	VSUB	O	High Voltage Output (2 level : VHH, VEE)	
16	VHH	-	Power (15V)	

2. Absolute Maximum Ratings (Ta=25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	VHH	-0.3 ~ VEE +29	V
	VME	VEE -0.3 ~ 3.0	
	VEE	0 ~ -10	
Input Voltage	VI	-0.3 ~ VHH +0.3	
Output Voltage	ΦV1,ΦV2,ΦV3,ΦV4,VSUB	VEE -0.3 ~ VHH +0.3	
Operating Temperature	T_{OPR}	-20 ~ +85	mA
Storage Temperature	T_{STG}	-45 ~ +120	°C

3. Logic Function Table

INPUT				OUTPUT		
XV1,3	XSG1,3	XV2,4	XSUB	ΦV1,3	ΦV2,4	VSUB
L	L	-	-	VHH	-	-
H	L	-	-	Z	-	-
L	H	-	-	VME	-	-
H	H	-	-	VEE	-	-
-	-	L	-	-	VME	-
-	-	H	-	-	VEE	-
-	-	-	L	-	-	VHH
-	-	-	H	-	-	VEE

4. AC Characteristics

(VHH=15V, VME=GND, VEE=-8.5V ; Ta=25°C)

Description	Symbol	Test Condition	Min	Typ	Max	Unit
Delay Time	TPLM	No Load (*1)	10	40	70	ns
	TPMH	No Load (*1)	10	30	70	
	TPLH	No Load (*1)	10	40	100	
	TPML	No Load (*1)	10	100	200	
	TPHM	No Load (*1)	10	100	180	
	TPHL	No Load (*1)	10	60	100	
Rising Time	TTLM	VEE → VME (*1)	400	700	930	
	TTMH	VME → VHH (*1)	400	650	930	
	TTLH	VEE → VHH (*1)	10	50	100	
Falling Time	TTML	VME → VEE (*1)	200	300	500	
	TTHM	VHH → VME (*1)	400	600	820	
	TTHL	VHH → VEE (*1)	10	50	100	
Output Noise Voltage	VCLH, VCLL VCMH, VCML	(*2)	-	-	0.5	V

(*1) Refer Timing Diagram

(*2) Refer Noise Diagram

5. DC Characteristics

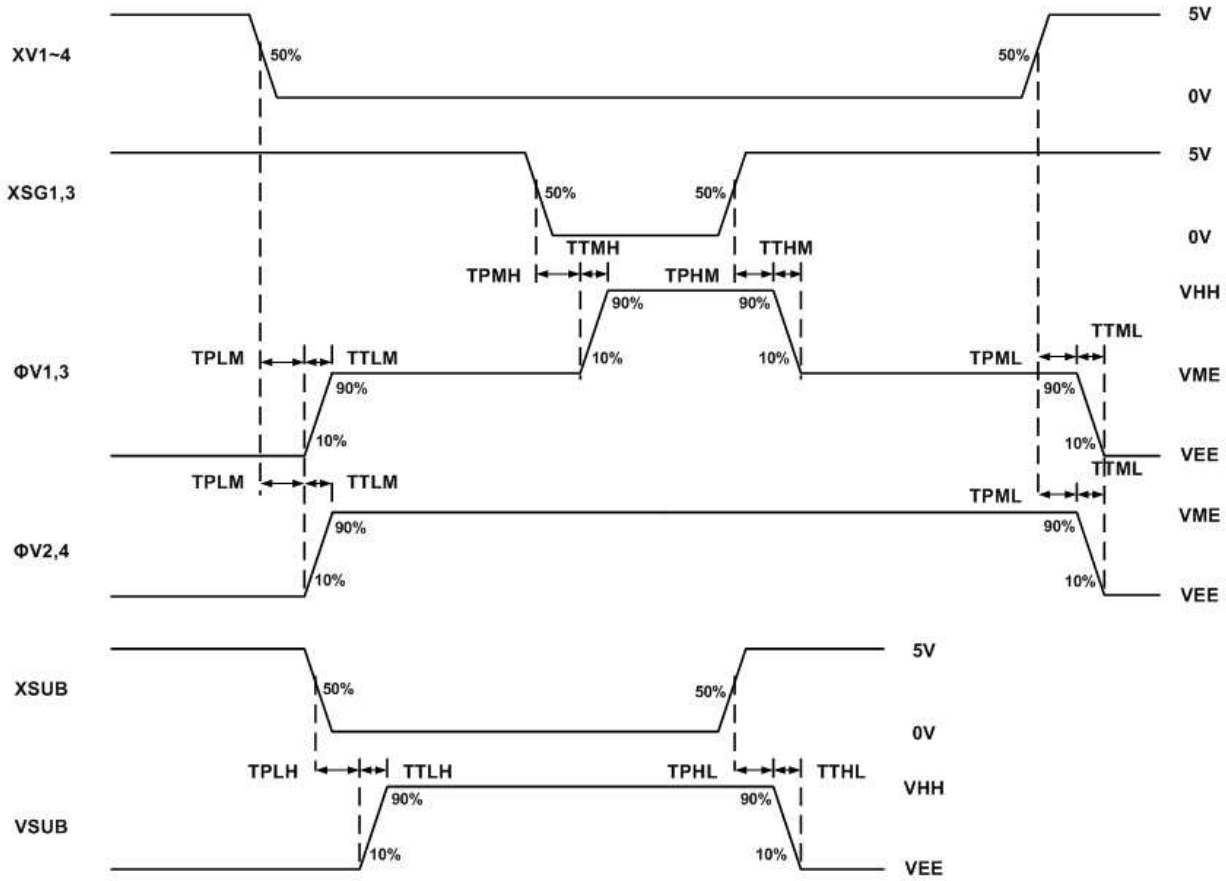
(VHH=15V, VME=GND, VEE=-8.5V ; Ta=25°C)

Description	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	VHH		14.5	15	15.5	V
	VEE		-9.5	-8.5	-7.5	
High Level Input Voltage	VIH	(*3)	2.3	-	-	
Low Level Input Voltage	VIL	(*3)	-	-	1.2	
Input Current	II	VIN = 0 ~ 5V (*3)	-1.0	0.0	1.0	uA
Operation Current	IHH	(*4)	-	2.0	3.5	mA
	IME	(*4)	-	4.5	5.0	
	IEE	(*4)	-8.5	-6.5	-	
Output Current	IOL	ΦV1~4 = -8.0V	25	37	-	
	IOM1	ΦV1~4 = -0.5V	-	-15	-10	
	IOM2	ΦV1,3 = 0.5V	9	13.5	-	
	IOH	ΦV1,3 = 14.5V	-	-18	-12	
	IOSL	VSUB = -8.0V	12	18	-	
	IOSH	VSUB = 14.5V	-	-10.5	-7	

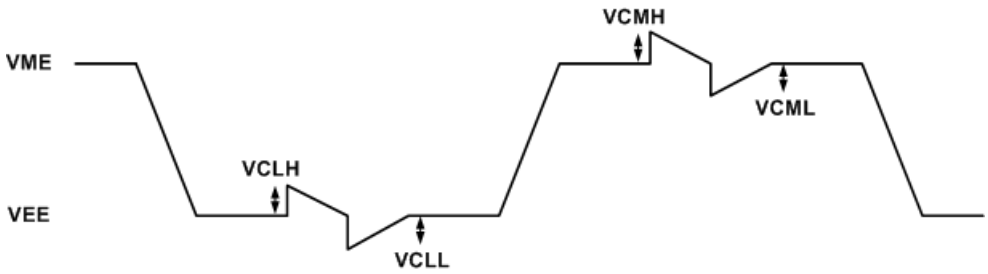
(*3) XV1~4, XSG1, XSG3, XSUB Pin

(*4) Refer the Test Circuit.

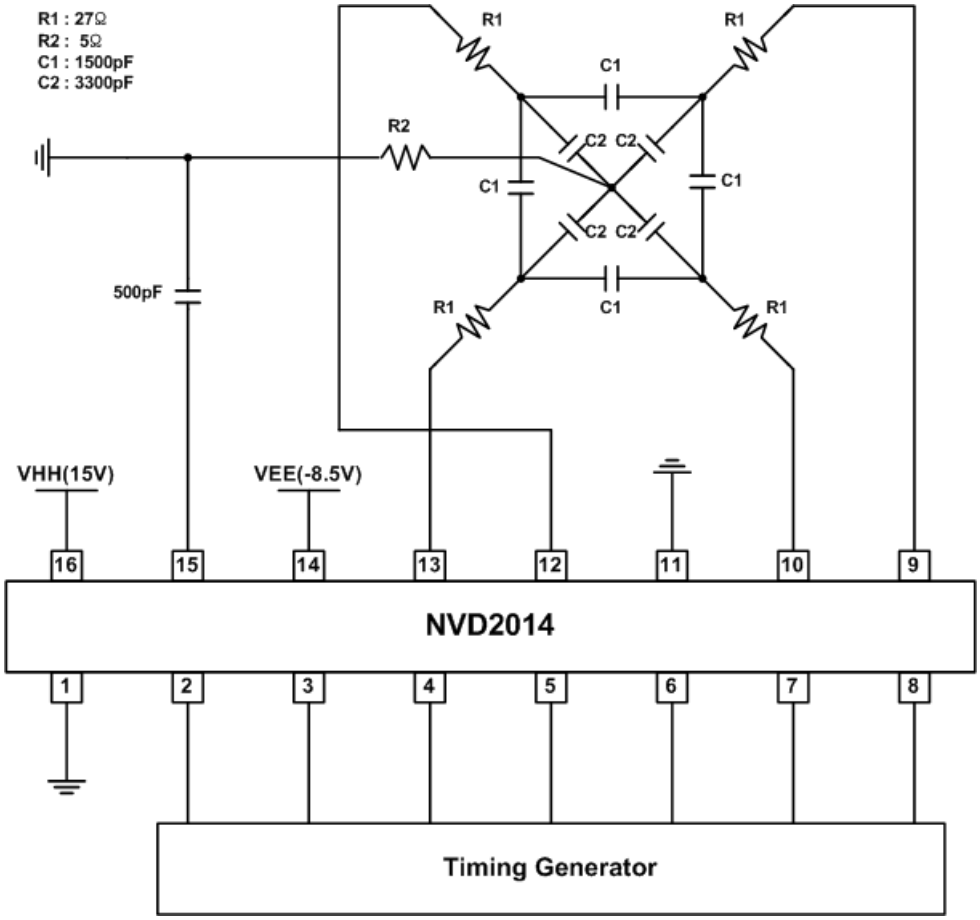
6. Timing Diagram



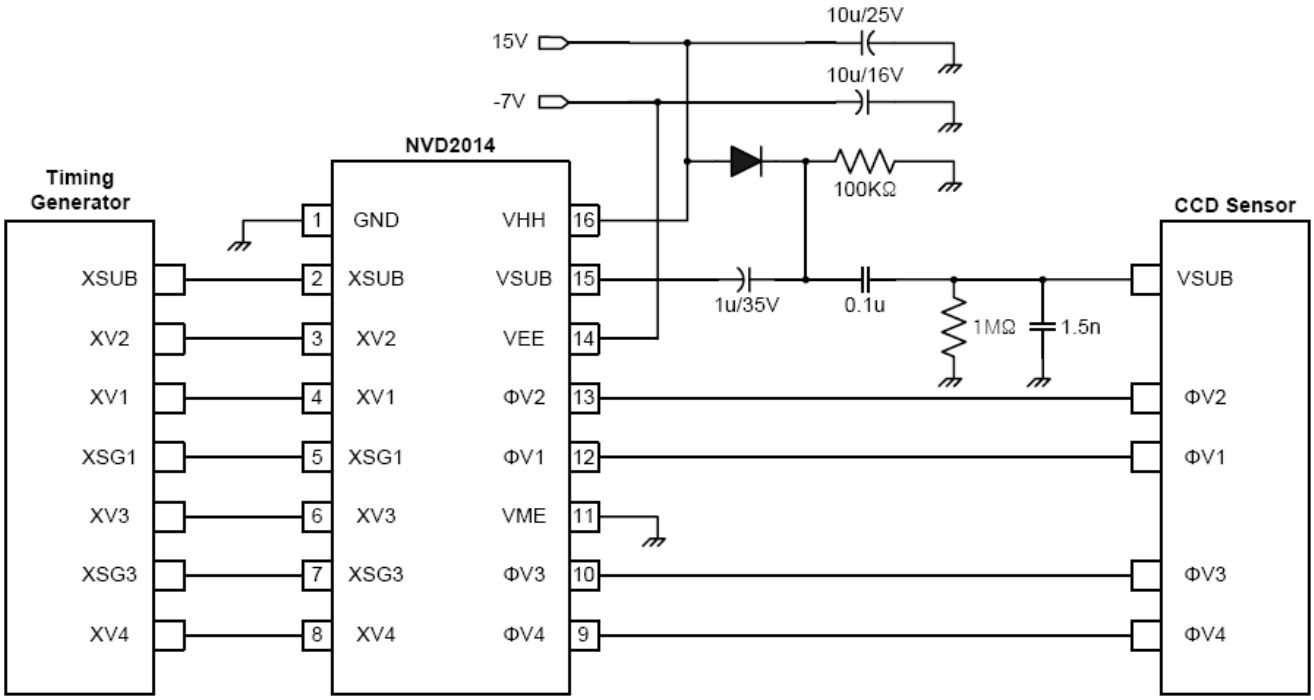
7. Noise Diagram



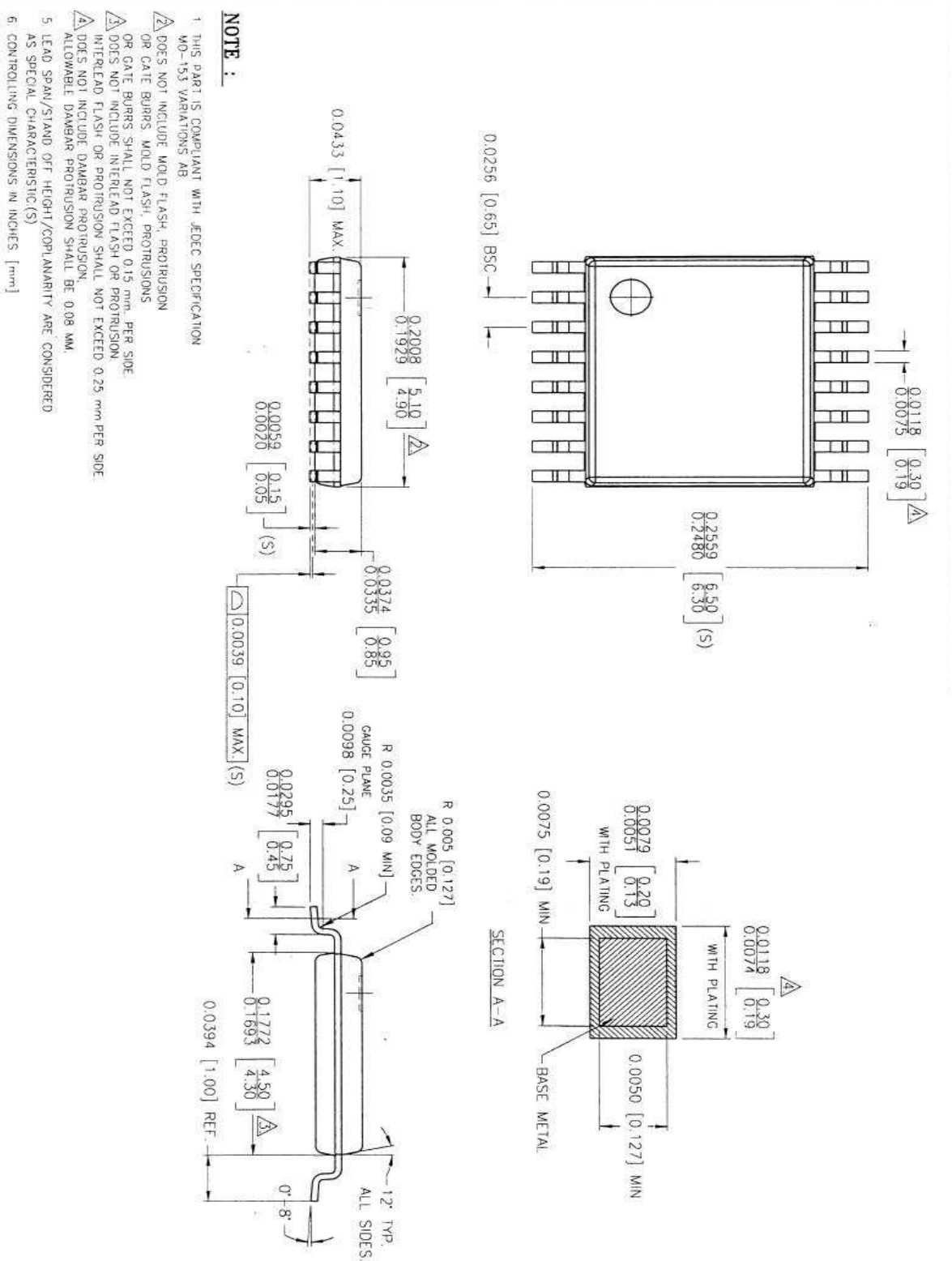
8. Test Circuit



9. Application Circuit (Example)



10. Package Dimension



11. Revision History

REV	Date	Description
Version 0.0	2006. 12. 13.	1st release

12. Contact Information

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